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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/752,879	12/28/2000	: Aditya Mukherjee	42390P9572X	9416	
8791	7590 10/23/2003		EXAMINER		
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD, SEVENTH FLOOR			LAMARRE	LAMARRE, GUY J	
	S ANGELES, CA 90025		ART UNIT	PAPER NUMBER	
,			2133		
			DATE MAILED: 10/23/2003	6	

Please find below and/or attached an Office communication concerning this application or proceeding.

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•	Application No.	Applicant(s)			
Office Assissa Community	09/752,879	MUKHERJEE, ADITYA			
Office Action Summary	Examin r	Art Unit			
71 1411 110 5 1 7 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Guy J. Lamarre, P.E.	2133			
Th MAILING DATE of this communication app ars on the cover shet with the correspondence address Period for Reply					
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status					
1) Responsive to communication(s) filed on 28 D	<u>ecember 2000</u> .				
2a)☐ This action is FINAL . 2b)⊠ Thi	s action is non-final.				
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. Disposition of Claims					
4)⊠ Claim(s) <u>1-20</u> is/are pending in the application.					
4a) Of the above claim(s) is/are withdrawn from consideration.					
5) Claim(s) is/are allowed.					
6)⊠ Claim(s) <u>1-20</u> is/are rejected.					
7) Claim(s) is/are objected to.					
8) Claim(s) are subject to restriction and/or election requirement.					
Application Papers					
9) The specification is objected to by the Examiner.					
10)⊠ The drawing(s) filed on <u>28 December 2000</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.					
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).					
11) The proposed drawing correction filed on is: a) approved b) disapproved by the Examiner.					
If approved, corrected drawings are required in reply to this Office action. 12)☐ The oath or declaration is objected to by the Examiner.					
Priority under 35 U.S.C. §§ 119 and 120					
<u> </u>					
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of:					
 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 					
3. Copies of the certified copies of the priority documents have been received in this National Stage					
application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.					
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).					
a) \square The translation of the foreign language provisional application has been received. 15) \square Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.					
Attachment(s)					
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)	5) Notice of Informal F	(PTO-413) Paper No(s) Patent Application (PTO-152)			

DETAILED ACTION

1. Applicant's pre-amendment of 20 Feb. 2001 and declaration of 9 Apr. 2001 have been entered.

- 1.1 Pursuant to 35 USC 131, Claims 1-20 are presented for examination.
- 1.2 The correction on page 10 line 8, as per pre-amendment of 20 Feb. 2001, has not been entered because the referenced passage cannot be found.

Claim Objections

2. The listed claims are objected to because of the following informalities:

Claim 3 line 2 should read "a second local control signal" instead of "a second local command signal." All other such occurrences of 'command' shall be corrected in said claim and other claims, e.g., Claims 4 and 18-19 to conform to language of respective last lines of independent Claims 1 and 16.

Double Patenting (non-statutory)

3. The non-statutory double patenting rejection, whether of the obviousness-type or non-obviousness-type, is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent. In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969); In re Vogel, 422 F.2d 438,164 USPQ 619 (CCPA 1970); In re Van Omum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985) and In re Goodman, 29 USPQ2d 2010 (Fed. Cir. 1993).

A timely filed terminal disclaimer in compliance with 3 7 CFR 1. 3 2 1 (b) and may be used to overcome an actual or provisional rejectin based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.78(d).

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Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3.1 Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over respective Claims 1-4 of copending US Patent application No. 09/677,392. Although the conflicting claims are not identical, they are not patentably distinct from each other.

The difference between instant claim 1 and the copending claims is the removal of a design for testability feature. It is well known and hence obvious that ICs are so designed. Those in possession of the invention would have been motivated to discard such design for testability feature in order to remove unnecessary limitations from the claim language so as to reduce cost and broaden scope of patent protection.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC ' 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

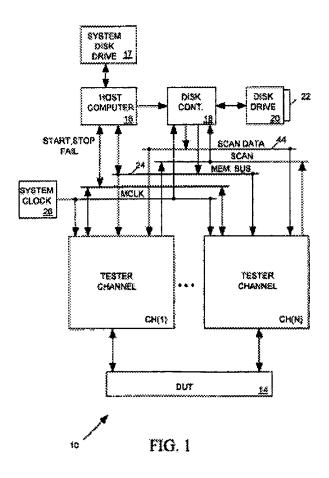
A person shall be entitled to a patent unless –

- (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.
- 4.1 Claims 1-20 are rejected under 35 U.S.C. 102 (e) as being anticipated by Wasson (US Patent No. 6,181,151; Oct. 28, 1998 (filing date)).

Wasson anticipates the claimed invention because Wasson teaches, e.g., in Abstract: "An integrated circuit (IC) tester includes set of tester channels, each for carrying out a test Application/Control Number: 09/752,879

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activity at a separate terminal of an IC device under test (DUT) during each cycle of a test. The tester also includes a disk drive having a removable disk for reading out scan or programming data to the tester channels during a test. Each tester channel includes an instruction memory for storing a set of instructions, and each tester channel executes its stored instructions during the test. Some of the instructions include VECTOR data directly indicating a particular test activity the tester channel is to carry out at a DUT terminal during a next test cycle. Others of the instructions tell the tester channel to acquire a particular number (N) of serial data bits as they are read out of the disk drive and to carry out an activity during each of the next N test cycles indicated by a state of a corresponding one of the N serial data bits."

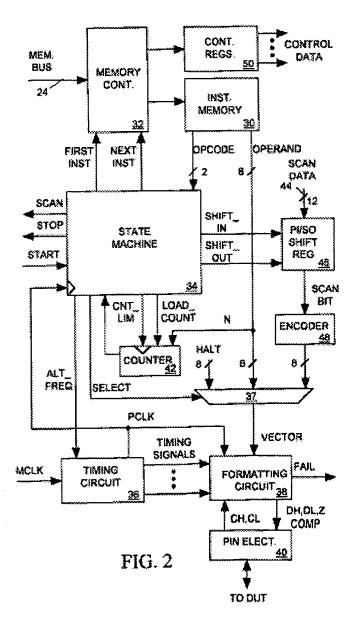


As per Claims 1, 6, 11, 16, Wasson depicts, in Figs. 1-2 and related description in col. 1 line 10 et seq., the claimed apparatus or system or means circuit comprising: internal data bus

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(col. 2 line 55, or Fig. 1 numeral 24); plural clusters coupled to said bus (Fig. 1 CH1..CHN); test controller coupled to said bus (col. 4 line 45 or col. 6 line 50 et seq., as seen in Fig. 1 Blocks 16 and 18); and a debug or tester or tester unit coupled to said bus (col. 4 line 47 et seq.) wherein the bus is configured to generate system or global control signal (at col. 4 lines 46 et seq.) and each of said plural clusters configured to generate local or separate control signals at col. 4 lines 49 et seq.



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As per Claims 2, 17, Wasson depicts, in Fig. 2 and related description in col. 4 line 55 et seq., the claimed timing or sync or deskew buffer or memory means (Fig. 2 timing circuit 36) along with local clock driving means effected by Fig. 2 formatting circuit 38 as described in col. 5 line 27 et seq.

As per Claims 3, 7, 12, 18, Wasson depicts, in Fig. 2 and related description in col. 5 line 27 et seq., equivalent test control distribution means.

As per Claims 4, 8, 13, 19, Wasson depicts, in Fig. 2 and related description in col. 5 line 27 et seq., equivalent snapshot instruction and shift instruction means, e.g., in Fig. 2 block 46 and col. 6 line 2-3, 43 et seq.

As per Claims 5, 9, 14, 20, Wasson depicts, in Fig. 2 and related description in col. 5 line 27 et seq., equivalent snapshot instruction and shift instruction means, e.g., in Fig. 2 block 46 and col. 6 line 2-3, 43 et seq.

As per Claim 10, 15, Wasson depicts, in Fig. 2 and related description in col. 6 line 62 et seq., the claimed debug or test triggering means via variable time period under control of state machine 34 of Fig. 2.

4.2 To anticipate under section 102, a prior art reference must disclose all the elements of the claimed invention or their equivalents functioning in essentially the same way. The inquiry as to whether a reference anticipates a claim must focus on what subject matter is encompassed by the claim and what subject matter is described by the reference. As set forth by the court in *Kalman* v. *Kimberly-Clark Corp.* 713 F.2d 760, 218 USPQ 781, 789 (Fed. Cir. 1983), cert. denied, 465 U.S. 1026 (1984) it is only necessary for the claims to "read on' something disclosed in the reference, i.e., all limitations in the claim are found in the reference, or 'fully met' by it." The Examiner respectfully submits that all the limitations of Claims 1-20, or their equivalents functioning in essentially the same way, are found in the Wasson reference.

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Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The references cited in Form PTO-892 are for the Applicant's review.

5.1 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306, for formal communications intended for entry

Or: (703) 746-5463, for informal or draft communications, please label "PROPOSED" or "DRAFT."

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (703) 305-0755. The examiner can normally be reached on Monday to Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady, can be reached on (703) 305-9595.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Guy J. Lamarre, P.E.

Gry J. Lamarre

Patent Examiner

10/15/03